JC780 U.S. PTO
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UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new non-provisional applications under 37 CFR 1.53(b)

Attorney Docket No. 42390.P6156 Total Pages 2

First Named Inventor or Application Identifier Carole Dulong

Express Mail Label No. EL431886484US

JC690 U.S. PTO
09/538012
03/29/00

ADDRESS TO: **Assistant Commissioner for Patents**
Box Patent Application
Washington, D. C. 20231

APPLICATION ELEMENTS
See MPEP chapter 600 concerning utility patent application contents.

1. X Fee Transmittal Form
(Submit an original, and a duplicate for fee processing)

2. X Specification (Total Pages 18)
(preferred arrangement set forth below)
- Descriptive Title of the Invention
- Cross References to Related Applications
- Statement Regarding Fed sponsored R & D
- Reference to Microfiche Appendix
- Background of the Invention
- Brief Summary of the Invention
- Brief Description of the Drawings (if filed)
- Detailed Description
- Claims
- Abstract of the Disclosure

3. X Drawings(s) (35 USC 113) (Total Sheets 11)

4. X Oath or Declaration (Total Pages 5)

a. ___ Newly Executed (Original or Copy)

b. ___ Copy from a Prior Application (37 CFR 1.63(d))
(for Continuation/Divisional with Box 17 completed) **(Note Box 5 below)**

i. ___ DELETIONS OF INVENTOR(S) Signed statement attached deleting inventor(s) named in the prior application, see 37 CFR 1.63(d)(2) and 1.33(b).

5. ___ Incorporation By Reference (useable if Box 4b is checked)
The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied under Box 4b, is considered as being part of the disclosure of the accompanying application and is hereby incorporated by reference therein.

6. ___ Microfiche Computer Program (Appendix)

7. ___ Nucleotide and/or Amino Acid Sequence Submission

(if applicable, all necessary)

a. ____ Computer Readable Copy
b. ____ Paper Copy (identical to computer copy)
c. ____ Statement verifying identity of above copies

ACCOMPANYING APPLICATION PARTS

8. _____ Assignment Papers (cover sheet & documents(s))
9. _____ a. 37 CFR 3.73(b) Statement (where there is an assignee)

_____ b. Power of Attorney

10. _____ English Translation Document (if applicable)
11. _____ a. Information Disclosure Statement (IDS)/PTO-1449

_____ b. Copies of IDS Citations

12. _____ Preliminary Amendment
13. X___ Return Receipt Postcard (MPEP 503) (Should be specifically itemized)
14. _____ a. Small Entity Statement(s)

___ b. Statement filed in prior application, Status still proper and desired

15. _____ Certified Copy of Priority Document(s) (if foreign priority is claimed)

16. Other: _____

_____

_____

_____

17. **If a CONTINUING APPLICATION,** check appropriate box and supply the requisite information:

___ Continuation ____ Divisional ____ Continuation-in-part (CIP)

of prior application No: _____

18. **Correspondence Address**

_____ Customer Number or Bar Code Label _____
(Insert Customer No. or Attach Bar Code Label here)

or

__X__ Correspondence Address Below

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043290.P6156 *Patent*

UNITED STATES PATENT APPLICATION

for

METHOD AND APPARATUS FOR VECTOR GATHER AND SCATTER

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Attorney's Docket No. 042390.P6156

"Express Mail" mailing label number EL431886484US

Date of Deposit March 29, 2000

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(typed or printed name of person mailing paper or fee)

Cindy Murphy
(Signature of person mailing paper or fee)

METHOD AND APPARATUS FOR VECTOR GATHER AND SCATTER

BACKGROUND OF THE INVENTION

Field of the Invention

This invention relates generally to the field of processor operations. More particularly, the invention relates to an apparatus and method for performing vector gather and scatter operations using a computer processor.

Description of the Related Art

In order to perform vector computations on a computer, matrices such as that illustrated in **Figure 1** must frequently be loaded into memory. Once in memory, the matrix may be combined with other matrices (not shown) to perform complex, multidimensional computations (e.g., vector addition, vector multiplication).

One problem which exists, however, is that matrices can take up a substantial amount of memory, particularly when used to store certain types of data (e.g., scientific data pertaining to physical phenomenon). In addition, matrices may be sparsely populated with data elements. For example, only 4 data elements out of the 24 illustrated in **Figure 1** contain non-zero values, resulting in an inefficient use of memory.

To conserve memory when working such large, sparsely populated matrices, "gather" and "scatter" operations were developed. For example, the

CRAY-1 computer system performed gather operations to collect the elements of a matrix from memory and store them in a highly compressed format (e.g., sorted contiguously in an ordered array). Conversely, when necessary to perform various matrix operations (e.g., matrix multiplication) the CRAY-1 performed scatter operations to reproduce the previously-gathered matrix in memory.

One problem which exists, however, is that these systems require complex dedicated hardware to perform the gather and scatter operations. For example, the CRAY-1 employed a vector processor which performed gather and scatter operations using dedicated registers to hold index vectors and dedicated address calculation hardware.

Accordingly, what is needed is a more efficient apparatus and method for storing and working with matrices in a computing environment. What is also needed is a system and method for performing gather and scatter operations on a general purpose processor.

BRIEF DESCRIPTION OF THE DRAWINGS

A better understanding of the present invention can be obtained from the following detailed description in conjunction with the following drawings, in which:

FIG. 1 illustrates matrix with data elements which may be stored in a computer memory.

FIG. 2 illustrates an exemplary computer architecture used to implement elements of the invention.

FIG. 3 illustrates a variety of data and data storage formats according to embodiments of the invention.

FIG. 4 illustrates extract and deposit operations according to embodiments of the invention.

FIG. 5 illustrates one embodiment of a method for performing a gather operation.

FIG. 6 illustrates the extraction of a set of address indices according to one embodiment of the invention.

FIG. 7 illustrates address calculation and storage operations according to one embodiment of the invention.

FIG. 8 illustrates memory load operations according to one embodiment of the invention.

FIG. 9 illustrates the merging of data elements in a register according to one embodiment of the invention.

FIG. 10 illustrates one embodiment of a method for performing a scatter operation.

FIG. 11 illustrates performing an extract operation on a plurality of data elements according to one embodiment of the invention.

DETAILED DESCRIPTION

In the following description, for the purposes of explanation, numerous specific details are set forth in order to provide a thorough understanding of the present invention. It will be apparent, however, to one skilled in the art that the present invention may be practiced without some of these specific details. In other instances, well-known structures and devices are shown in block diagram form to avoid obscuring the underlying principles of the present invention.

Embodiments of the present invention include various steps, which will be described below. The steps may be embodied in machine-executable code. The instructions can be used to cause a general-purpose or special-purpose processor to perform certain steps. Alternatively, these steps may be performed by specific hardware components that contain hardwired logic for performing the steps, or by any combination of programmed computer components and custom hardware components.

AN EXEMPLARY COMPUTER SYSTEM

Figure 2 shows a computer system 200 upon which embodiments of the invention may be implemented. Computer system 200 comprises a bus 201 for communicating information, a processor 210 coupled to the bus 201 for processing information, and a memory subsystem 204-206 coupled to bus 201 for storing information and instructions for the processor 210. The memory

subsystem may be comprised of a main memory 204, a read only memory 206 and/or a mass storage device 205.

The processor 210 includes an execution unit 230, a register file 250, a cache memory 260, a decoder 265, and an internal bus 270. The cache memory 260, storing frequently and/or recently used information for the processor 210, is coupled to the execution unit 230. Register file 250 is comprised of a group of registers for storing data to be read by the execution unit 230 via the internal bus 270. In one embodiment, the registers within the register file 250 store sixty-four bits of packed data for integer and/or floating point calculations.

The execution unit 230 operates on packed data according to the instructions received by processor 210 that are included in a packed instruction set 240. The execution unit 230 also operates on non-packed data according to instructions implemented in general-purpose processors. In one embodiment the processor 210 is an Explicitly Parallel Instruction Computing ("EPIC") processor (e.g., employing the IA-64 parallel architecture developed by Intel®), capable of executing multiple instructions per clock cycle. In addition, processor 210 in one embodiment is capable of supporting the Intel Itanium™ microprocessor instruction set as well as the packed instruction set 240. Other instruction sets, such as the Pentium®, PowerPC™ and the Alpha® processor instruction sets may also be used in accordance with the described invention. Pentium and Itanium are trademarks of Intel Corporation. PowerPC™ is a trademark of IBM,

APPLE COMPUTER, and MOTOROLA. Alpha™ is a trademark of Digital Equipment Corporation.

Still referring to **Figure 2**, computer system 200 can also be coupled to a second I/O bus 250 via an I/O interface 230. A plurality of I/O devices may be coupled to I/O bus 250, including, for example, a display device 243, an alphanumeric input device 242 (e.g., a keyboard), a cursor control device 241 and/or a communication device 240. The communication device 240 is for accessing other computers and may comprise a modem, a network interface card, or other well known interface device, such as those used for coupling to Ethernet, token ring, or other types of networks.

DATA AND STORAGE FORMATS

Figure 3 illustrates three packed data-types: packed byte 301, packed word 302, and packed doubleword (dword) 303. Packed byte 301 is sixty-four bits long containing eight packed byte data elements. Generally, a data element is an individual piece of data that is stored in a single register (or memory location) with other data elements of the same length. In packed data sequences, the number of data elements stored in a register is the register size (e.g., 64-bits in the embodiment illustrated in **Figure 3**) divided by the length in bits of a data element. Although the registers illustrated in **Figure 3** and described throughout the specification are 64-bit registers, it should be noted that the underlying principles of the invention may be implemented on registers of virtually any size.

EXTRACT AND DEPOSIT OPERATIONS

Figures 4a and **4b** illustrate two data operations which may be used in one embodiment of the invention. As illustrated in **Figure 4a**, an "extract" operation involves copying a specified bit field from a source register R_S to an aligned position within a destination register R_D (i.e., the least significant bit (LSB) of the bit field is aligned with bit zero of the destination register R_D). Conversely, a "deposit" operation, as illustrated in **Figure 4b**, copies a specified bit field from an aligned position in a source register R_S to a specified location within a destination register R_D.

In one embodiment, individual extract and deposit instructions are included in the packed instruction set 240. Accordingly, the extract instruction may be used to copy a data element from a source register to an aligned position in a destination register. For example, the instruction EXTR $R_D = R_S$, 32, 16 copies a data element 16 bits in length located at bit 32 in the source register (i.e., the LSB of the data element is positioned at bit 32 of the source register) to an aligned position in a destination register as illustrated in **Figure 4a**.

Similarly, a deposit instruction may be used to copy a data element aligned in a source register to a specified position in a destination register. For example, the instruction DEP $R_D = R_D$, R_S, 16, 32, copies a 16 bit data element aligned in a source register to a position starting at bit 32 (i.e., the LSB of the data element is aligned with bit 32 of the destination register as illustrated in **Figure**

4b). In this embodiment, the R_D designation to the right of the equal sign indicates that data elements stored in the remaining bit positions of the destination register should not be overwritten (e.g., with zeros). As described below, this feature allows a series of packed data elements to be merged into a single register.

GATHER OPERATION

In one embodiment of the apparatus and method, extract and deposit operations are used to perform "gather" operations in which non-zero data elements of a matrix are retrieved (i.e., "gathered") from memory and stored in a contiguous manner.

As set forth in the flowchart in **Figure 5**, in one embodiment, a plurality of address indices are extracted into an equal plurality of destination registers (at 510). Each of the indices, when combined with a base address, specifies an address in memory where a matrix data element is stored. For example, as illustrated in **Figure 6**, four indices I0, I1, I2, and I3 packed in a single register, R3, are extracted into four individual registers, R5, R8, R11, and R14, respectively. Four extract instructions (e.g., EXTR R5 = R3, 0, 16 for I0) may be executed to perform this operation. In the particular embodiment illustrated in **Figure 6** each of the indices are 16-bits in length. However, it should be noted that indices of varying lengths may also be used in accordance with the underlying principles of the invention.

Addresses for each of the data elements are then computed at 520 (**Figure 5**) by adding each of the indices to the base address stored in R2. Thus, in the embodiment illustrated in **Figure 7**, the base address is added to each of the indices in R5, R8, R11, and R14 and the result (i.e., the addresses in memory of each of the data elements) are stored in registers R6, R9, R12 and R15, respectively.

The processor 210, at 530 (**Figure 5**), then loads the data elements from memory into a group of registers. For example, in the embodiment illustrated in **Figure 8**, data elements E0, E1, E2, and E3 are loaded from memory (after being identified via the calculated addresses) into registers R7, R10, R13 and R16, respectively.

At 540 (**Figure 5**), the data elements are merged into a single register. In one embodiment, this is accomplished using deposit operations. For example, referring to **Figure 9**, a series of deposit operations copy, in succession, E0, E1, E2, and E3 into register R4. The end result is that data elements E0-E3, which may have been scattered throughout a matrix, are now stored contiguously in register R4 (and/or a mass storage device), thereby preserving a substantial amount of memory.

SCATTER OPERATION

The matrix containing data elements E0-E3 may need to be reconstructed in memory from time to time so that matrix operations can be performed (e.g., matrix multiplication, addition . . . etc). In one embodiment, a "scatter" operation is used to carry out this function. Referring to **Figure 10**, in one embodiment of the scatter operation, indices are extracted (at 1010) and added to a base address to compute the addresses in memory to which the data elements will be scattered (at 1020). This portion of the scatter operation may be similar to the first portion of the gather operation described above (e.g., 510, 520 of **Figure 5**).

At 1030 the data elements are extracted from the register into which they were merged. Thus, as illustrated in **Figure 11**, each of the data elements E0, E1, E2 and E3 are extracted from register R4 and copied into registers R7, R10, R13, and R16, respectively (e.g., for element E2 the extract instruction might read EXTR R13 = R4, R13, 32, 16). Finally, at 1040, the data elements are stored to memory based on their previously-calculated addresses. A store instruction such as STORE [R12] = R13 may be executed by the processor 210 to perform this function (i.e., the data element from R13 is stored to the memory location found in R12).

Throughout the foregoing description, for the purposes of explanation, numerous specific details were set forth in order to provide a thorough

understanding of the invention. It will be apparent, however, to one skilled in the art that the invention may be practiced without some of these specific details. Accordingly, the scope and spirit of the invention should be judged in terms of the claims which follow.

5

CLAIMS

What is claimed is:

1. A method for performing a gather operation on a computer processor comprising:

computing addresses for one or more data elements of a matrix stored in memory;

loading each of said data elements into separate storage locations; and

depositing each of said data elements contiguously in a single storage location.

2. The method as in claim 1 wherein said storage locations are registers.

3. The method as in claim 1 wherein computing addresses comprises:

extracting indices for each of said data elements into separate storage locations; and

adding each of said indices to a base address.

4. The method as in claim 1 wherein depositing each of said data elements is accomplished via a DEPOSIT instruction executed by said computer processor.

5. The method as in claim 4 wherein said computer processor executes multiple DEPOSIT instructions in a single clock cycle.

6. The method as in claim 1 further comprising:

storing each of said data elements on a mass storage device.

7. The method as in claim 2 wherein said registers are 64-bits wide and said data elements are 16-bits in length.

8. A method for performing a scatter operation on a computer processor comprising:

calculating addresses in memory to which a plurality of data elements are to be scattered to form a matrix in memory;

extracting each of said data elements from a storage location in which said elements are stored contiguously; and

storing said data elements to said addresses in memory.

9. The method as in claim 8 wherein said storage location is a register.

10. The method as in claim 8 wherein computing addresses comprises:

extracting indices for each of said data elements into separate storage locations; and

adding each of said indices to a base address.

11. The method as in claim 8 wherein extracting each of said data elements is accomplished via an EXTRACT instruction executed by said computer processor.

12. The method as in claim 11 wherein said computer processor executes multiple EXTRACT instructions in a single clock cycle.

13. The method as in claim 9 wherein said register is 64-bits wide and said data elements are 16-bits in length.

14. A computer system comprising:

a memory;

a processor communicatively coupled to the memory; and

a storage device communicatively coupled to the processor and having stored therein a sequence of instructions which, when executed by the processor, causes the processor to at least,

compute addresses for one or more data elements of a matrix stored in memory;

load each of said data elements into separate storage locations; and

deposit each of said data elements contiguously in a single storage location.

15. The computer system as in claim 14 wherein said storage locations are registers.

16. The computer system as in claim 14 wherein, responsive to one or more instructions in said sequence, said processor computes addresses by:

extracting indices for each of said data elements into separate storage locations; and

adding each of said indices to a base address.

17. The computer system as in claim 14 wherein depositing each of said data elements is accomplished via a DEPOSIT instruction executed by said processor.

18. The computer system as in claim 17 wherein said processor executes multiple DEPOSIT instructions in a single clock cycle.

19. The computer system as in claim 14 wherein, responsive to one or more instructions in said sequence, said processor further:

stores each of said data elements on said mass storage device.

20. The computer system as in claim 15 wherein said registers are 64-bits wide and said data elements are 16-bits in length.

ABSTRACT

A processor and computer system are described which execute gather and scatter operations with general purpose instructions. Gather operations comprise identifying non-zero data elements of a matrix stored in memory and depositing the data elements contiguously within a register (e.g., in a packed data format). Scatter instructions comprise extracting the data elements packed contiguously within a register or memory and copying the elements to identified non-contiguous locations in a matrix stored in memory.

.243	0	0	0	1.542	0
0	0	0	0	0	0
0	0	0	0	0	0
0	0	0	0	0	0
0	0	0	0	.256	0
0	.020	0	0	0	0

FIG. 1

006250 "2708560

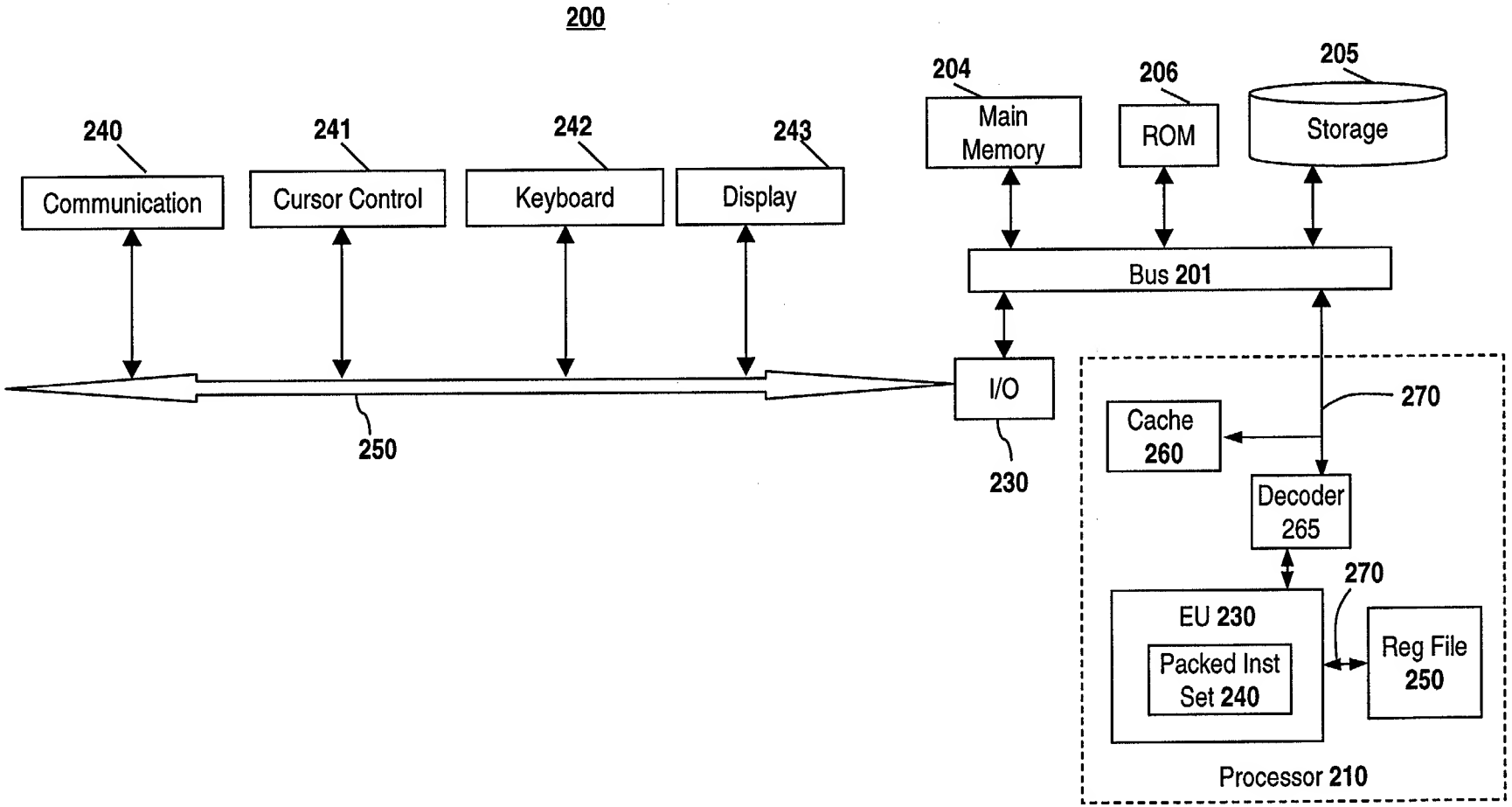


FIG. 2

006250" 2708560

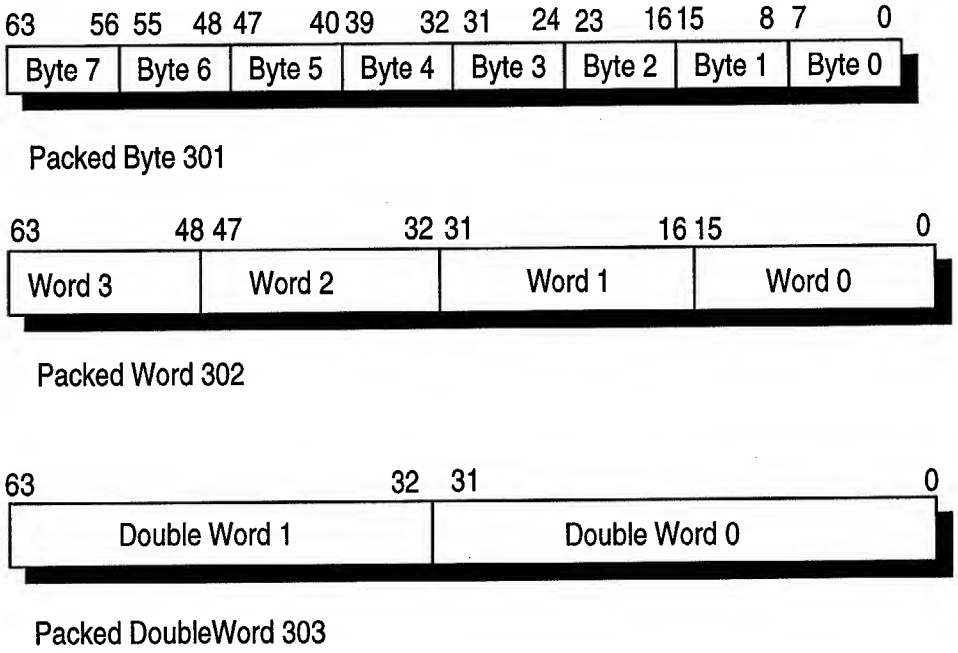
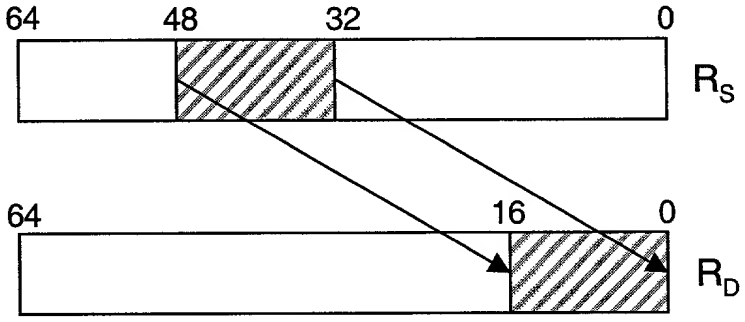
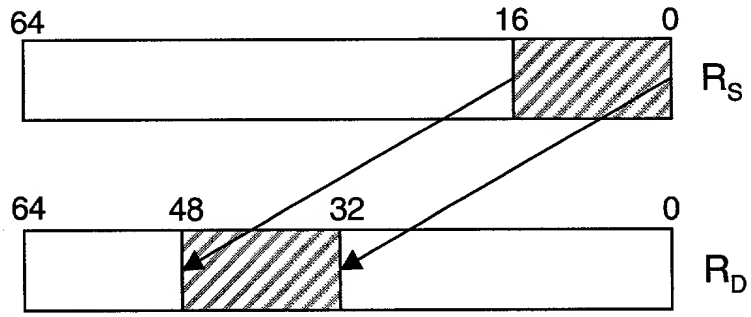


FIG. 3



Extract

FIG. 4a



Deposit

FIG. 4b

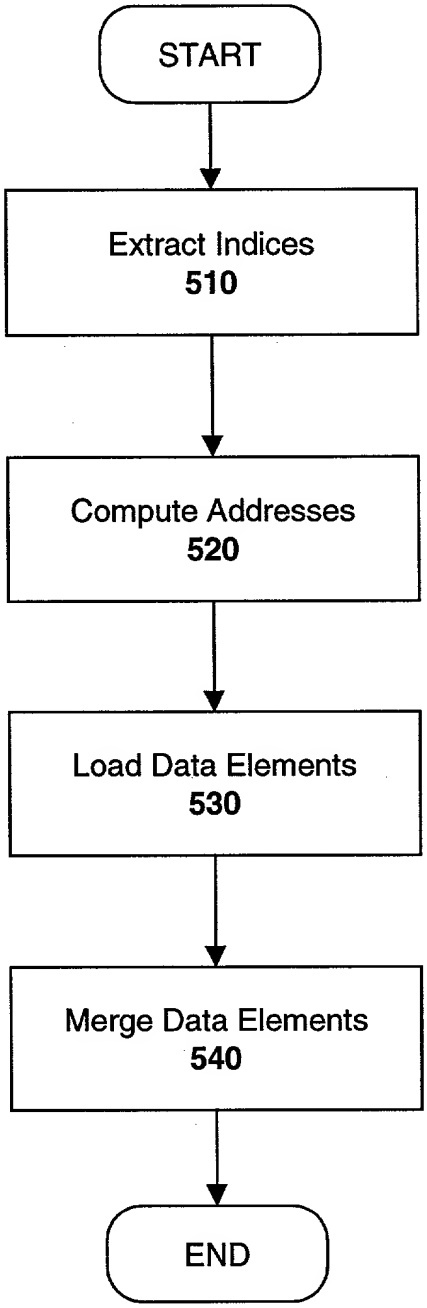

START
Extract Indices
510
Compute Addresses
520
Load Data Elements
530
Merge Data Elements
540
END

FIG. 5

0062E0" 2708E560

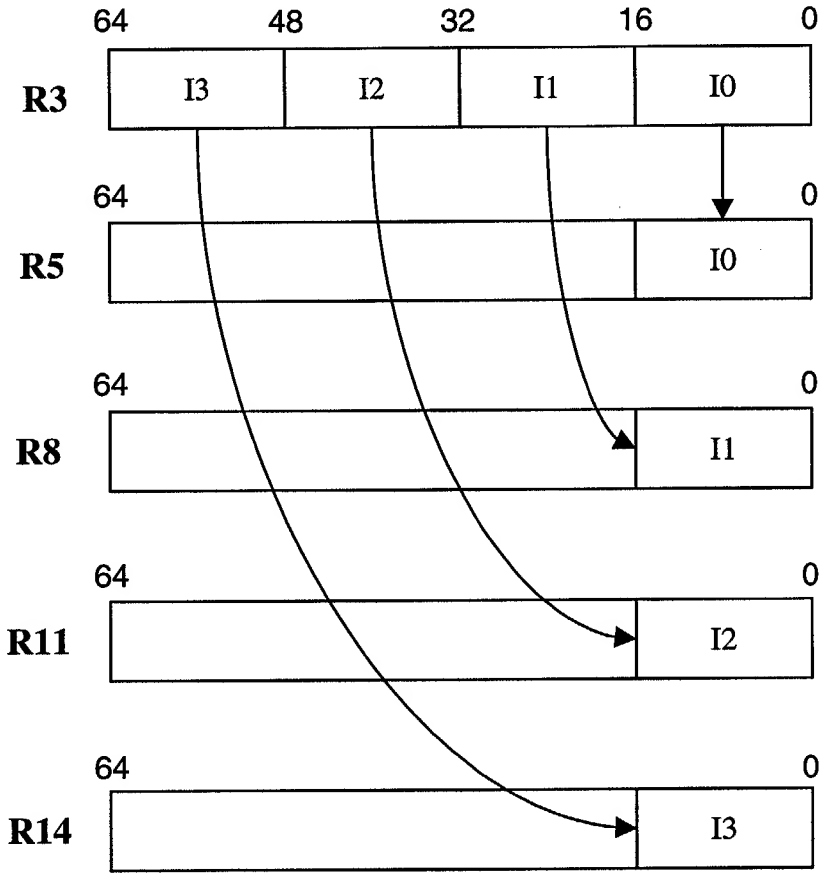


FIG. 6

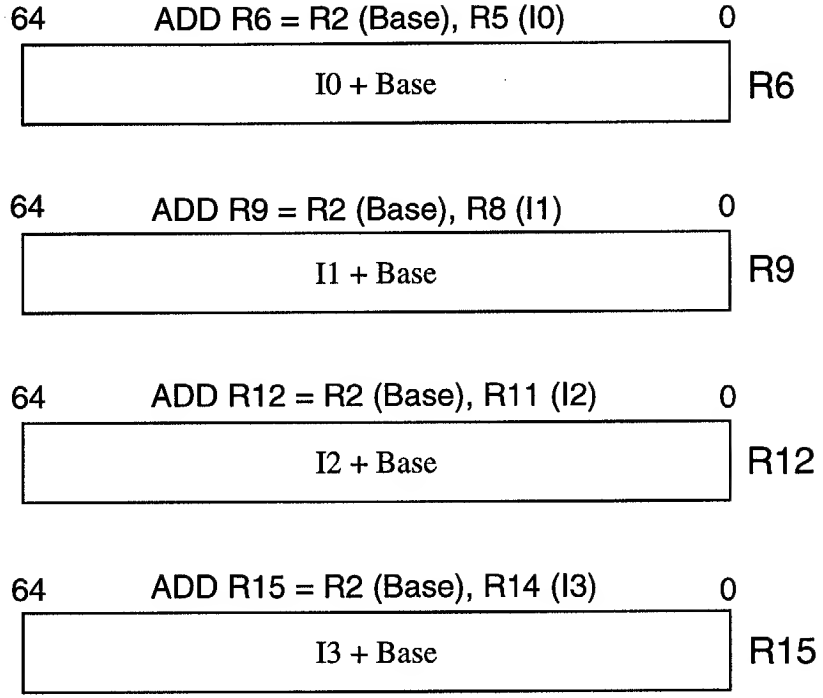

64
ADD R6 = R2 (Base), R5 (I0)
0
I0 + Base
R6
64
ADD R9 = R2 (Base), R8 (I1)
0
I1 + Base
R9
64
ADD R12 = R2 (Base), R11 (I2)
0
I2 + Base
R12
64
ADD R15 = R2 (Base), R14 (I3)
0
I3 + Base
R15

FIG. 7

006260 "27085560

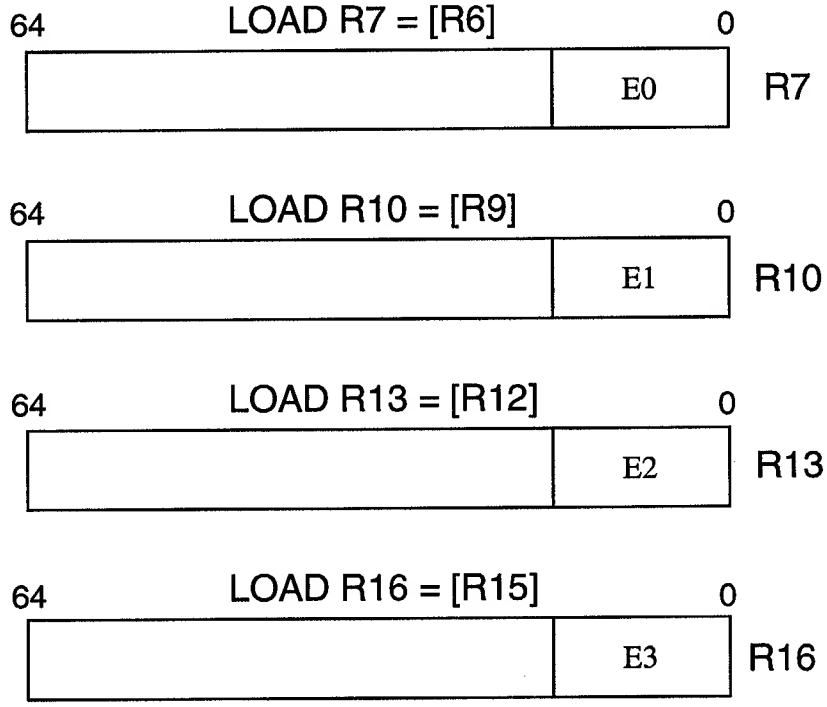


FIG. 8

006250" 2708560

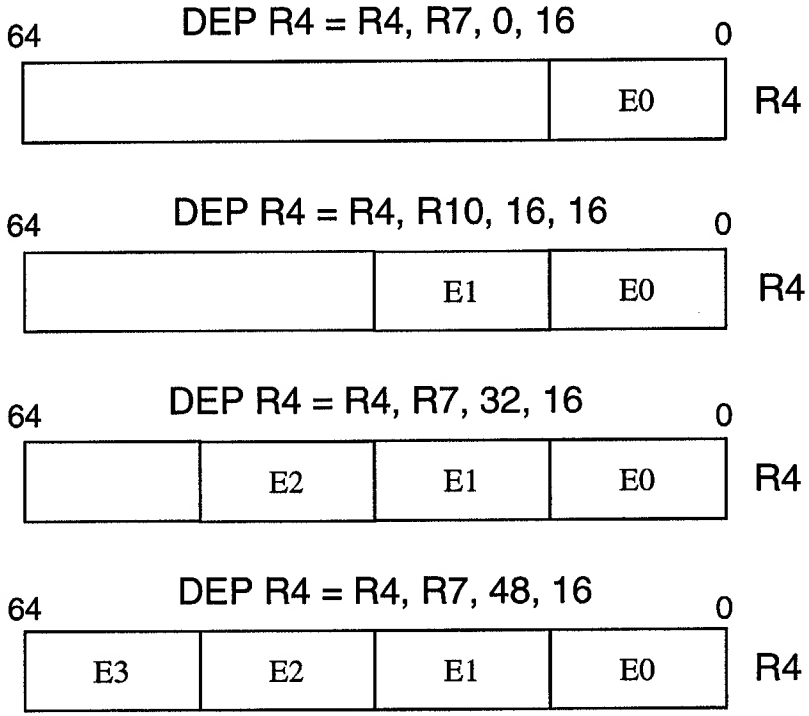


FIG. 9

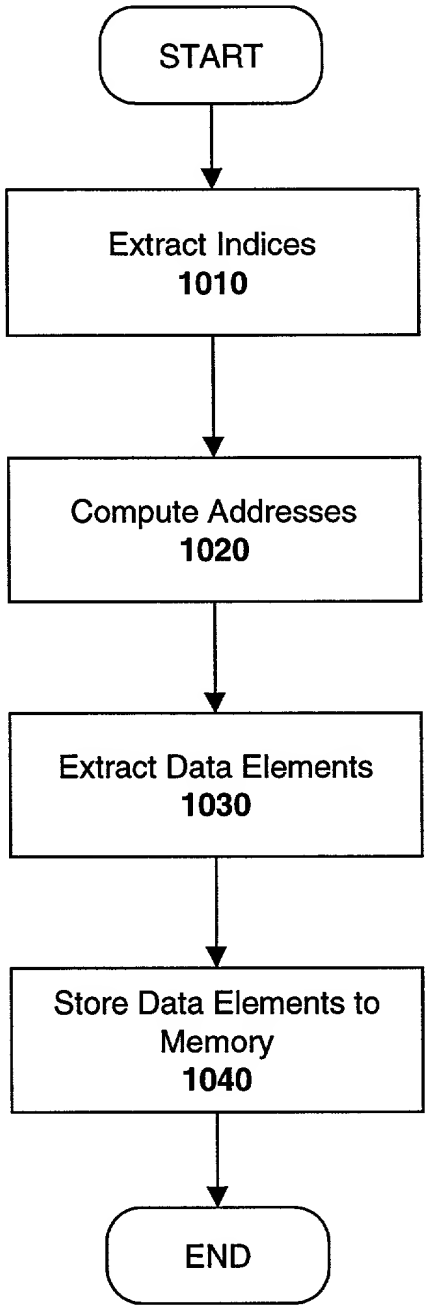

START
Extract Indices
1010
Compute Addresses
1020
Extract Data Elements
1030
Store Data Elements to Memory
1040
END

FIG. 10

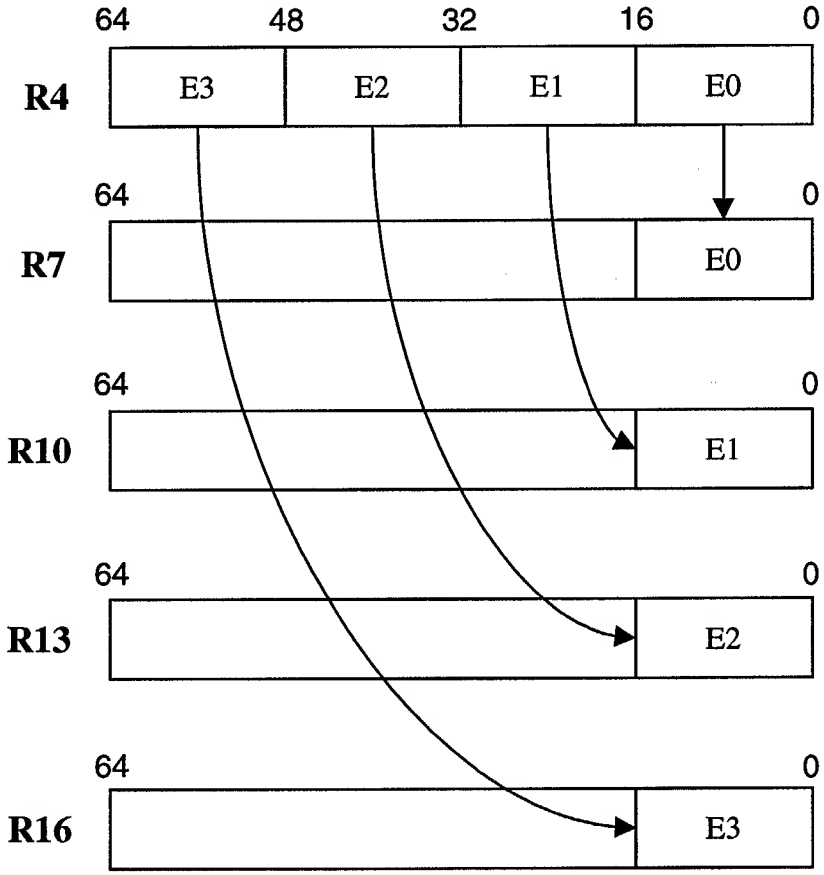

64
48
32
16
0
R4
E3
E2
E1
E0
64
0
R7
E0
64
0
R10
E1
64
0
R13
E2
64
0
R16
E3

FIG. 11

Attorney's Docket No.: 42390.P6156 PATENT

DECLARATION AND POWER OF ATTORNEY FOR PATENT APPLICATION
(FOR **INTEL CORPORATION** PATENT APPLICATIONS)

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below, next to my name.

I believe I am the original, first, and sole inventor (if only one name is listed below) or an original, first, and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

Method And Apparatus For Vector Gather And Scatter

the specification of which

_X_ is attached hereto.
___ was filed on _____ as
United States Application Number _____
or PCT International Application Number_____
and was amended on _____.
(if applicable)

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claim(s), as amended by any amendment referred to above. I do not know and do not believe that the claimed invention was ever known or used in the United States of America before my invention thereof, or patented or described in any printed publication in any country before my invention thereof or more than one year prior to this application, that the same was not in public use or on sale in the United States of America more than one year prior to this application, and that the invention has not been patented or made the subject of an inventor's certificate issued before the date of this application in any country foreign to the United States of America on an application filed by me or my legal representatives or assigns more than twelve months (for a utility patent application) or six months (for a design patent application) prior to this application.

I acknowledge the duty to disclose all information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56.

I hereby claim foreign priority benefits under Title 35, United States Code, Section 119(a)-(d), of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

Prior Foreign Application(s)			Priority Claimed	
(Number)	(Country)	(Day/Month/Year Filed)	Yes	No
(Number)	(Country)	(Day/Month/Year Filed)	Yes	No
(Number)	(Country)	(Day/Month/Year Filed)	Yes	No

I hereby claim the benefit under Title 35, United States Code, Section 119(e) of any United States provisional application(s) listed below:

Application Number	Filing Date
Application Number	Filing Date

I hereby claim the benefit under Title 35, United States Code, Section 120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, Section 112, I acknowledge the duty to disclose all information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56 which became available between the filing date of the prior application and the national or PCT international filing date of this application:

Application Number	Filing Date	Status -- patented, pending, abandoned
Application Number	Filing Date	Status -- patented, pending, abandoned

I hereby appoint the persons listed on Appendix A hereto (which is incorporated by reference and a part of this document) as my respective patent attorneys and patent agents, with full power of substitution and revocation, to prosecute this application and to transact all business in the Patent and Trademark Office connected herewith.

Send correspondence to Thomas C. Webster **(Name of Attorney or Agent), BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP, 12400 Wilshire Boulevard 7th Floor, Los Angeles, California 90025 and direct telephone calls to** Thomas C. Webster **(Name of Attorney or Agent), (408) 720-8300.**

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

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APPENDIX A

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APPENDIX B

Title 37, Code of Federal Regulations, Section 1.56
Duty to Disclose Information Material to Patentability

(a) A patent by its very nature is affected with a public interest. The public interest is best served, and the most effective patent examination occurs when, at the time an application is being examined, the Office is aware of and evaluates the teachings of all information material to patentability. Each individual associated with the filing and prosecution of a patent application has a duty of candor and good faith in dealing with the Office, which includes a duty to disclose to the Office all information known to that individual to be material to patentability as defined in this section. The duty to disclosure information exists with respect to each pending claim until the claim is cancelled or withdrawn from consideration, or the application becomes abandoned. Information material to the patentability of a claim that is cancelled or withdrawn from consideration need not be submitted if the information is not material to the patentability of any claim remaining under consideration in the application. There is no duty to submit information which is not material to the patentability of any existing claim. The duty to disclosure all information known to be material to patentability is deemed to be satisfied if all information known to be material to patentability of any claim issued in a patent was cited by the Office or submitted to the Office in the manner prescribed by §§1.97(b)-(d) and 1.98. However, no patent will be granted on an application in connection with which fraud on the Office was practiced or attempted or the duty of disclosure was violated through bad faith or intentional misconduct. The Office encourages applicants to carefully examine:

(1) Prior art cited in search reports of a foreign patent office in a counterpart application, and

(2) The closest information over which individuals associated with the filing or prosecution of a patent application believe any pending claim patentably defines, to make sure that any material information contained therein is disclosed to the Office.

(b) Under this section, information is material to patentability when it is not cumulative to information already of record or being made or record in the application, and

(1) It establishes, by itself or in combination with other information, a prima facie case of unpatentability of a claim; or

(2) It refutes, or is inconsistent with, a position the applicant takes in:

(i) Opposing an argument of unpatentability relied on by the Office, or

(ii) Asserting an argument of patentability.

A prima facie case of unpatentability is established when the information compels a conclusion that a claim is unpatentable under the preponderance of evidence, burden-of-proof standard, giving each term in the claim its broadest reasonable construction consistent with the specification, and before any consideration is given to evidence which may be submitted in an attempt to establish a contrary conclusion of patentability.

(c) Individuals associated with the filing or prosecution of a patent application within the meaning of this section are:

(1) Each inventor named in the application;

(2) Each attorney or agent who prepares or prosecutes the application; and

(3) Every other person who is substantively involved in the preparation or prosecution of the application and who is associated with the inventor, with the assignee or with anyone to whom there is an obligation to assign the application.

(d) Individuals other than the attorney, agent or inventor may comply with this section by disclosing information to the attorney, agent, or inventor.